Modulation Strategies for Direct-Link Drive for Open-End Winding AC Machines

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***Abstract*—Switching common-mode voltages generated by conventional pulse-width modulated inverters are known to cause bearing currents in ac machines. These undesirable currents may result in bearing damage. A direct-link drive for open-end winding ac machines has recently been proposed. Some advantages of the drive include: 1) common-mode voltage suppression, 2) no storage elements, and 3) ability to achieve up to 1.5 times the peak input phase voltage across the machine phase windings. In this paper, pulsewidth modulation strategies for the drive are proposed. Two strategies are based on space vector modulation and suppress common-mode voltage at the machine terminals. One carrier-based strategy achieves 1.5 times the peak input phase voltage across the machine phase windings but causes switching common-mode voltage at the machine terminals. Simulation and experimental results are presented to verify the operation of the drive.**

I. Introduction

Pulse-width modulated (PWM) inverters are widely used in variable frequency drives. However, conventional PWM inverters cause switching common-mode voltages at the terminals of ac machines. These switching common-mode voltages are known to cause undesirable bearing currents which may damage the machine bearings [1] [2]. EMI issues also arise due to these common-mode voltages [3]. Methods have been proposed in literature which address this problem. Extra hardware or special modulation strategies are employed to reduce common-mode voltages [4]–[6].

In [7], a direct-link drive for open-end winding ac machines was proposed. The drive has the advantages of:

1) No energy storage components
2) Ability to achieve up to 1.5 times the peak input phase voltage across the machines phase windings
3) Suppression of common-mode voltages at the machine terminals

This topology combined the benefits of the topologies presented in [8] and [9]. In addition to the above advantages, the drive uses 18 unidirectional switches as compared to 36 switches used by the matrix converter based drives in [10] and [11].

Operation of the direct-link drive has been presented in [7]. It is briefly outlined again in Section II. Section III presents three modulation strategies for the direct-link drive. Simulation and experimental results for the drive are presented in Sections IV and V respectively.

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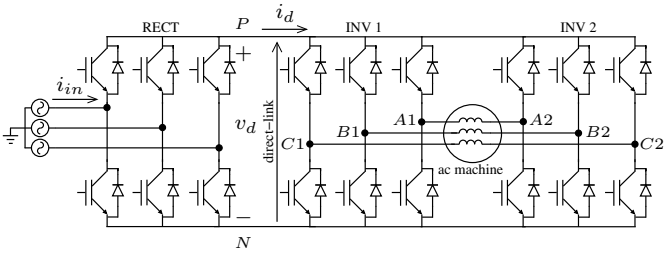

Fig. 1. Direct-link drive for open-end winding ac machines

II. Direct-Link Drive and Its Operation

The circuit configuration of the direct-link drive is shown in Fig. 1. The front-end rectifier is denoted by 'RECT'. Its operation is similar to that of a three-phase diode bridge rectifier. Switches (e.g. IGBT's) with bidirectional current carrying capability are used instead of diodes to allow operation in the generating mode. The top-switch of a phase leg is turned ON when the corresponding phase voltage is maximum. Similarly, the bottom switch is turned ON when the corresponding phase voltage is minimum. The direct-link voltage (v_d in Fig. 1) is a three-phase line-rectified voltage. This is shown in Fig. 2. Also, the input current of the direct-link drive (i_{in}) is a $120°$-conduction waveform with unity displacement power factor. The input power factor of the drive is uncontrollable and the input current has considerable total harmonic distortion (THD $\approx 30\%$).

The two inverters, shown as 'INV1' and 'INV2' in Fig. 1, are modulated in synchronism to generate three-phase sinusoidal voltages across the machine phase windings. Due to high switching frequencies of modern drives ($5-20$ kHz), the time-varying nature of the direct-link voltage v_d poses no problem. It has been shown in [7] and [9] that using only certain active vectors of the two inverters, common-mode voltage at the terminals of the ac machine can be limited to a slowly varying waveform. The common-mode voltage is proportional to the direct-link voltage and therefore varies at 360 Hz for a drive with 60 Hz input voltages. This voltage does not have any high frequency components. Thus it is expected that it will not cause any undesirable bearing currents.

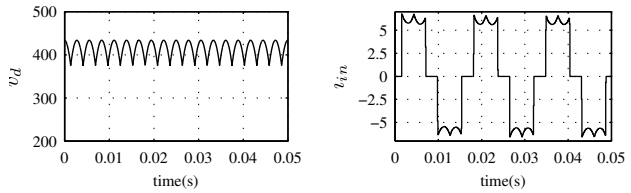

Fig. 2. (a) Direct-link voltage for direct-link drive (b) Input current for direct-link drive

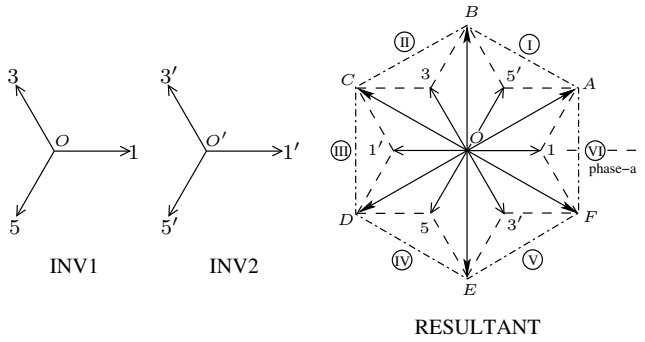

Fig. 3. Resultant space vectors across open-end windings

III. Modulation of Direct-Link Drive

The common-mode voltage generated at the terminals of the ac machine can be defined as:

$$v_{CM1} = \frac{v_{A1N} + v_{B1N} + v_{C1N}}{3}$$
$$v_{CM2} = \frac{v_{A2N} + v_{B2N} + v_{C2N}}{3} \quad (1)$$

It has been shown in [7] and [9] that by using only certain active vectors of the individual inverters, common-mode voltage can be suppressed. In Fig. 3, vectors $1, 3$ and 5 have a common-mode voltage of $v_d/3$. Vectors $2, 4$ and 6 have a common-mode voltage of $2v_d/3$. If only vectors $1, 3, 5$ and $1', 3', 5'$ are used to generate the output voltage, the common-mode voltage at the machine terminals will always be $v_d/3$ [9]. The resultant vectors that appear across the machine phase windings are $OA, OB, \ldots$ and OF. These are shown in Fig. 3. Using these vectors for output voltage generation does not cause any switching common-mode voltage the the machine terminals.

A. Space vector based modulation strategy

The resultant vectors across the open end-windings that do not cause any switching common-mode voltage are shown in Fig. 3. The resultant zero vectors are obtained by applying vectors combinations $1-1'$, $3-3'$ and $5-5'$. In sector I, to generate the output voltage vector, vectors OA and OB are applied along with the zero vector in a switching time period. To apply the effective vector OA, INV1 should apply vector 1 and INV2 should apply vector $5'$. Similarly, to generate vector OB, INV1 should apply vector 3 and INV2 should apply vector $5'$. To apply a zero vector, INV1 and INV2 should apply vectors 5 and $5'$ respectively. Thus it seen that in sector I, INV2 gets clamped to vector $5'$ and INV1 switches between the vectors 1, 3 and 5 [9].

In this modulation strategy, SVPWM is achieved using $OA, OB, \ldots$ and OF as basic vectors. The switching states are then mapped to the individual inverters INV1 and INV2. The resultant zero vectors are mapped to vectors of the individual vectors depending on the sector information. These mappings are shown in Tables I and II. While implementing space vector modulation on the resultant vectors, the vector lengths are not constant. This is due to the time-varying nature of the direct-link voltage v_d. The direct-link voltage thus needs to be sensed and compensated for. The time-varying voltage does not pose a problem in modulation due to high inverter switching frequencies and fast computational speeds [8].

It should be noted that the resultant vectors are shifted in the counter-clockwise direction with respect to the phase-a axis (Fig. 3). These vectors are rotated by $30°$. Thus the reference output voltage vector $(\vec{v}_{o,ref})$ also needs to be shifted by $30°$. Let the shifted reference voltage vector be denoted by $\vec{v}^*_{o,ref}$. Then,

$$\vec{v}^*_{o,ref} = \vec{v}_{o,ref} \quad e^{j30°} \quad (2)$$

B. Carrier-based modulation

A carrier-based PWM method for the direct-link drive is outlined here. This scheme is easy to implement. It is similar to conventional sine PWM of a three-phase two-level inverter. The control signals of the individual inverters are out of phase by $180°$. For a desired effective modulation index of m, the control signals for the two inverters are given by:

$$\begin{aligned} m_{A1} &= \frac{m}{2}\cos\omega t + \frac{1}{2} \\ m_{B1} &= \frac{m}{2}\cos\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{2} \\ m_{C1} &= \frac{m}{2}\cos\left(\omega t - \frac{4\pi}{3}\right) + \frac{1}{2} \\ m_{A2} &= -\frac{m}{2}\cos\omega t + \frac{1}{2} \\ m_{B2} &= -\frac{m}{2}\cos\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{2} \end{aligned} \quad (3)$$

TABLE I
Mapping of resultant vectors to individual inverters

Resultant Vector	OA	OB	OC	OD	OE	OF
INV1 Vector	1	3	3	5	5	1
INV2 Vector	$5'$	$5'$	$1'$	$1'$	$3'$	$3'$

TABLE II
Mapping of resultant zero vectors to individual inverters

Sector Number	I	II	III	IV	V	VI
INV1 Vector	5	3	1	5	3	1
INV2 Vector	$5'$	$3'$	$1'$	$5'$	$3'$	$1'$

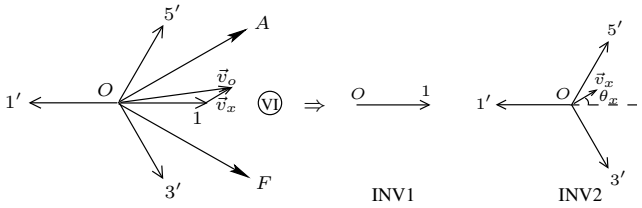

Fig. 4. Space vector modulation using difference vector

$$m_{C2} = -\frac{m}{2}\cos\left(\omega t - \frac{4\pi}{3}\right) + \frac{1}{2} \quad (4)$$

The effective control signals (for the voltages appearing across the machine phase windings) are thus given by:

$$\begin{aligned} m_{A1A2} &= m\cos\omega t \\ m_{B1B2} &= m\cos\left(\omega t - \frac{2\pi}{3}\right) \\ m_{C1C2} &= m\cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \quad (5)$$

The modulation index m can take a maximum value of 1. Thus the peak of the sinusoidal voltage that can be generated across the machine phase windings is $V_{d,min}$, where $V_{d,min}$ is the minimum direct-link voltage. Due the three-phase diode bridge like operation of the front-end, $V_{d,min} = 1.5\hat{V}_{ph}$. $\hat{V}_{ph}$ is the peak input phase voltage. Thus this modulation scheme also achieves 1.5 times the peak phase voltage across the machine phase windings. However, this modulation strategy does not address common-mode voltage elimination and switching common-mode voltages occur at the machine terminals. This scheme differs from conventional sine PWM with triplen harmonic injection in that no common-mode voltage is added in the machine phases. The common-mode voltage average in a switching cycle is zero and the circulating common-mode currents will be of switching frequency. Staggered carrier signals may be used in order to improve the voltage profile [12].

C. Space vector modulation using difference vector

It is seen in Fig. 3 that within each sector, one of the inverters gets clamped to one state and the other inverter switches between three states. This fact yields another modulation strategy. Here the difference between the desired output vector and the fixed vector is synthesized using the three vectors of the other inverter. As an example, in Fig. 4, the desired output vector is $\vec{v}_o$. INV1 is clamped to the vector 1. The difference vector, $\vec{v}_x$, is synthesized using INV2 vectors $1'$, $3'$ and $5'$. In the next sector INV2 will get clamped and INV1 vectors will be used to generate the difference vector. The switching time periods for the three active vectors of INV2 to generate $\vec{v}_x$ are given by,

$$\begin{aligned} \frac{T_{1'}}{T_s} &= \frac{1}{3} - \frac{2}{3}\, m_x \cos\theta_x \\ \frac{T_{3'}}{T_s} &= \frac{1}{3} - \frac{2}{3}\, m_x \cos\left(\theta_x - \frac{2\pi}{3}\right) \end{aligned}$$

$$\frac{T_{5'}}{T_s} = \frac{1}{3} - \frac{2}{3}\, m_x \cos\left(\theta_x - \frac{4\pi}{3}\right), \quad (6)$$

where T_s is the sampling period, m_x is the modulation index corresponding to $\vec{v}_x$ and θ_x is the position of $\vec{v}_x$.

IV. Simulation Results

The space vector and carrier-based techniques are simulated in Simulink®. The parameters for the simulation are given in Table III. The output voltage command is kept at 1.45 times the input voltage magnitude. For space vector based modulation, vector sets 1, 3 & 5 and $1'$, $3'$ & $5'$ were used for INV1 and INV2 respectively.

Fig. 5 shows the output phase voltage and current for space vector PWM based methods. The input phase voltage and current are shown in Fig. 6. The 120°-conduction nature of the input current is verified. The common-mode voltage at one of the machine terminals v_{CM1} and the common-mode voltage appearing across the machine phase windings are shown in Fig. 7. The common-mode voltage at the terminals is a slowly varying waveform. The frequency of variation is 360 Hz. Since it does not have any high dv/dt components, it is expected that this common-mode voltage will reduce harmful bearing currents as compared to conventional PWM drives. The common-mode voltage across the phase windings is zero.

Simulation results for the carrier-based PWM strategy are presented in Figs. 8-10. It is seen that switching common-mode voltages occur at the machine terminals when using this strategy. Common-mode voltage across the machine phase windings is also not zero. However, the switching cycle average of this voltage is zero and it does not cause any low frequency zero sequence currents.

V. Hardware Results

A 5kW prototype has been built and is shown in Fig. 11. Snubber capacitors (total combination of 1.98μF) are used across the direct-link to limit voltage spikes in the direct-link voltage v_d. The space vector modulation strategy is implemented on a dSPACE and FPGA-based system. PWM pulses from space vector modulation with the resultant vectors ($OA, OB, \ldots$ and OF) as basic vectors are generated within dSPACE. The mappings shown in Tables I and II are implemented in FPGA. The system parameters of the experimental setup are given in Table IV. The setup is operated at a lower power (about 1kW).

Fig. 12 shows the output phase voltage and current waveforms. The input phase voltage and current are shown in Fig. 13. The input current is 120°-conduction. The common-mode voltage at one of the terminals is shown in Fig. 14. It is seen

TABLE III
System Parameters used for simulation

Input phase voltage, v_{in}	$120V$ rms
Commanded output phase voltage, v_{out}	$174V$ rms
Three phase R-L load	$10\Omega, 10\ m$H
Switching frequency, f_{sw}	10 kHz

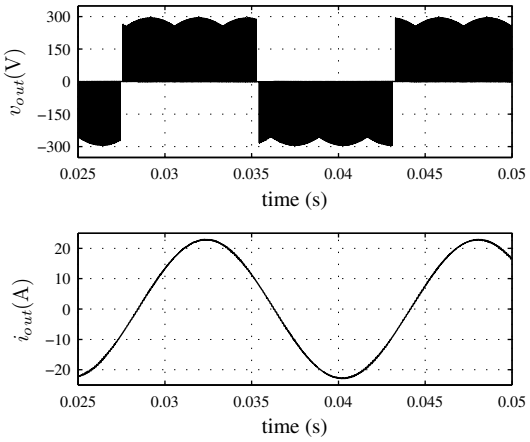

Fig. 5. Output phase voltage (v_{out}) and output phase current (i_{out}) for space vector-based PWM

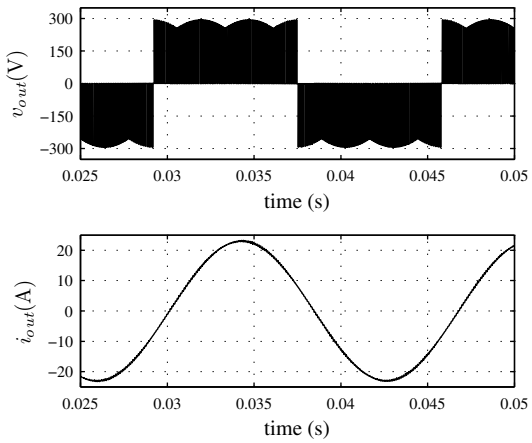

Fig. 8. Output phase voltage (v_{out}) and output phase current (i_{out}) for carrier-based PWM

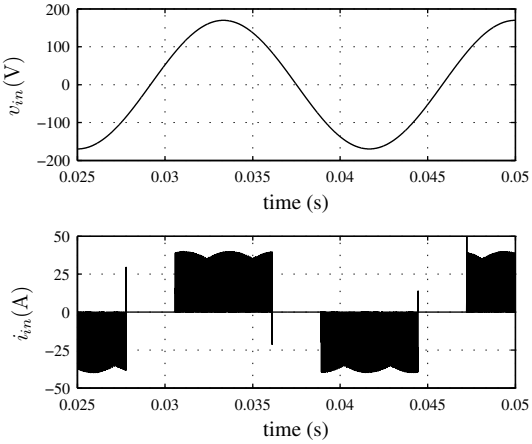

Fig. 6. Input phase voltage (v_{in}) and input phase current (i_{in}) for space vector-based PWM

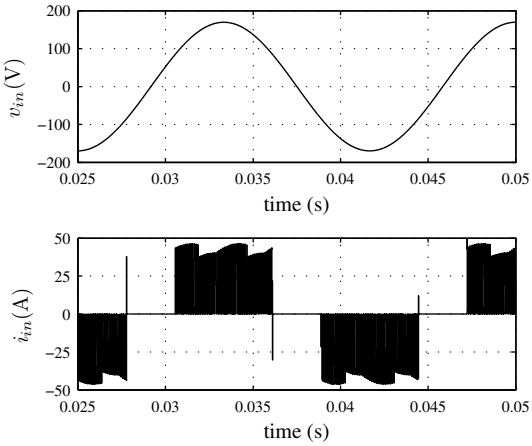

Fig. 9. Input phase voltage (v_{in}) and input phase current (i_{in}) for carrier-based PWM

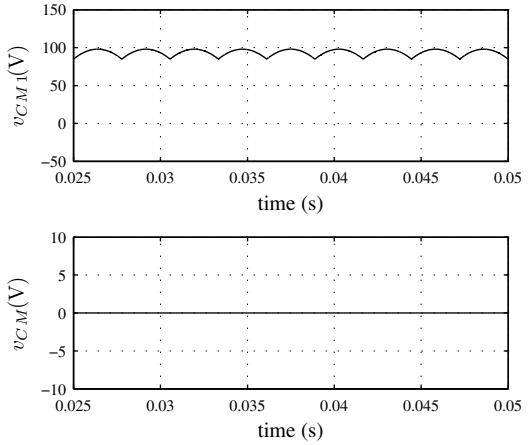

Fig. 7. Common-mode voltage at machine terminal (v_{CM1}) and across phase windings (v_{CM}) for space vector-based PWM

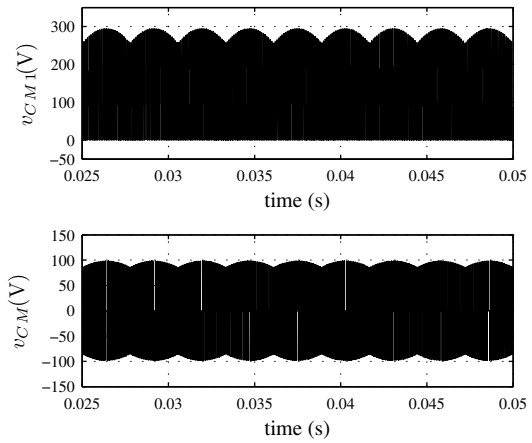

Fig. 10. Common-mode voltage at machine terminal (v_{CM1}) and across phase windings (v_{CM}) for carrier-based PWM

TABLE IV
SYSTEM PARAMETERS FOR EXPERIMENTAL SETUP

Input phase voltage, v_{in}	$70V$ rms
Commanded output phase voltage, v_{out}	$90V$ rms
Three phase R-L load	$22.5\Omega, 15\ m$H
Switching frequency, f_{sw}	5 kHz
Deadtime, T_d	5 μs

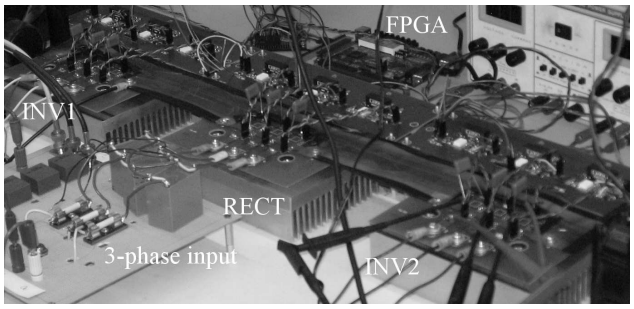

Fig. 11. Photograph of experimental setup

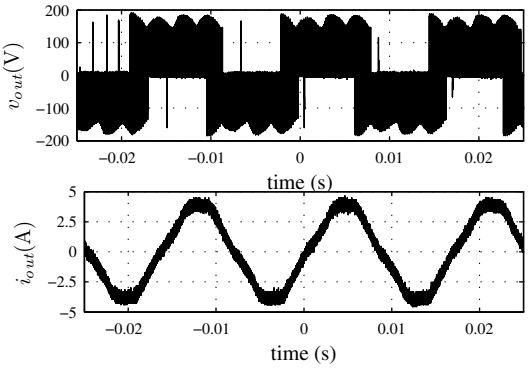

Fig. 12. Output phase voltage (v_{out}) and output phase current (i_{out}) for space vector-based PWM

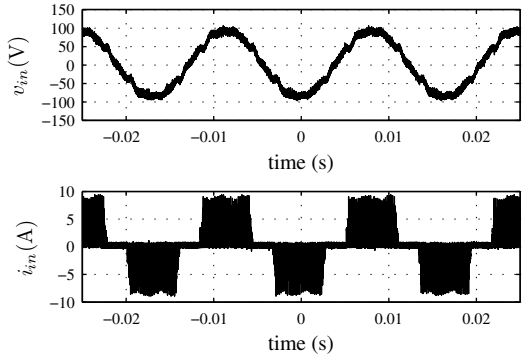

Fig. 13. Input phase voltage (v_{in}) and input phase current (i_{in}) for space vector-based PWM

that the common-mode voltage has switching components. This is due to deadtime used in the inverter legs and is evident in Fig. 15. A deadtime compensation scheme proposed in [13] can be employed to solve this problem.

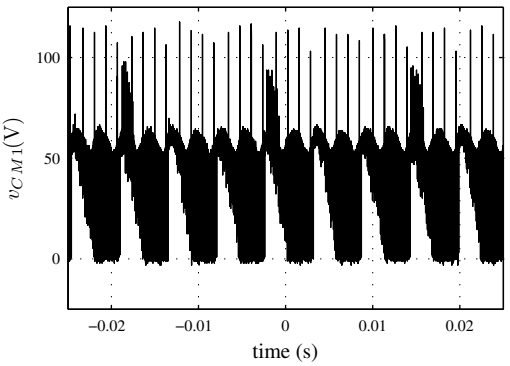

Fig. 14. Common-mode voltage at machine terminal for space vector-based PWM

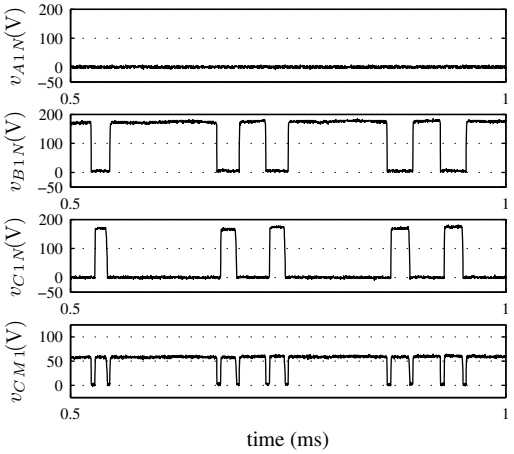

Fig. 15. Deadtime effect on common-mode voltage for space vector-based PWM

VI. CONCLUSION

Three modulation strategies for a direct-link drive for open-end winding machines have been presented. Two modulation strategies are space vector modulation based. These strategies do not cause any switching common-mode voltages at the machine terminals. A third carrier-based strategy is outlined which does not address the problem of switching common-mode voltage. All three strategies achieve up to 1.5 times the peak input phase voltage across the phase windings. Simulation and experimental results are presented.

REFERENCES

[1] J. M. Erdman, R. J. Kerkman, D. W. Schlelgel, and G. L. Skibinski, "Effect of pwm inverters on ac motor bearing currents and shaft voltages," *IEEE Trans. Appl. Ind.*, vol. 32, no. 2, pp. 250–259, 1996.

[2] S. Chen, T. A. Lipo, and D. Fitzgerald, "Source of induction motor bearing currents caused by pwm inverters," *IEEE Trans. Energy Convers.*, vol. 11, no. 1, pp. 25–32, Mar. 1996.

[3] S. Chen, T. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in pwm inverter drives," *Industry Applications, IEEE Transactions on*, vol. 32, no. 6, pp. 1365–1370, Nov/Dec 1996.

[4] R. S. Kanchan, P. N. Tekwani, M. R. Baiju, K. Gopakumar, and A. Pittet, "Three-level inverter configuration with common-mode voltage elimination for induction motor drive," *IEE Proceedings in Electric Power Applications*, vol. 152, no. 2, pp. 261–270, Mar. 2005.

[5] A. von Jounne, S. Dai, and H. Zhang, "A multilevel inverter approach providing dc-link balancing, ride-through enhancement, and common-mode voltage elimination," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 739–745, Aug. 2002.
[6] A. L. Julian, G. Oriti, and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 982–989, 1999.
[7] A. Somani, R. K. Gupta, T. Satish, and K. K. Mohapatra, "A pebb-based direct-link drive for open-ended ac machines," in *SCSC: Proceedings of the 2007 summer computer simulation conference*. San Diego, CA, USA: Society for Computer Simulation International, 2007, pp. 118–123.
[8] S. Kim, S.-K. Sul, and T. Lipo, "Ac/ac power conversion based on matrix converter topology with unidirectional switches," *IEEE Trans. Appl. Ind.*, vol. 36, no. 1, pp. 139–145, Jan/Feb 2000.
[9] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.
[10] K. Mohapatra and N. Mohan, "Open-end winding induction motor driven with matrix converter for common-mode elimination," *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, pp. 1–6, 12-15 Dec. 2006.
[11] K. K. Mohapatra and N. Mohan, "Open-end winding induction motor driven with indirect matrix converter for common-mode elimination," in *SCSC: Proceedings of the 2007 summer computer simulation conference*. San Diego, CA, USA: Society for Computer Simulation International, 2007, pp. 106–111.
[12] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Power Electronics and Applications, 1993., Fifth European Conference on*, Sep 1993, pp. 7–14 vol.5.
[13] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction pwm technique for inverter control with consideration of the dead-time effects-part i: basic development," *Industry Applications, IEEE Transactions on*, vol. 40, no. 6, pp. 1605–1612, Nov.-Dec. 2004.